module regi(clk,rst,sel,c1,c2,re1,re2,re3,cout1,result);

input clk,rst,c1,c2;

input [7:0]re1,re2,re3;

input [2:0]sel;

output reg cout1;

output reg [7:0]result;

always@(posedge clk)

begin

if(rst)

begin

result=8'd0;

cout1=1'd0;

end

else

begin

case(sel)

3'b000:begin result=re1; cout1=c1; end

3'b001:begin result=re2; cout1=c2; end

3'b011:begin result=re3; end

endcase

end

end

endmodule